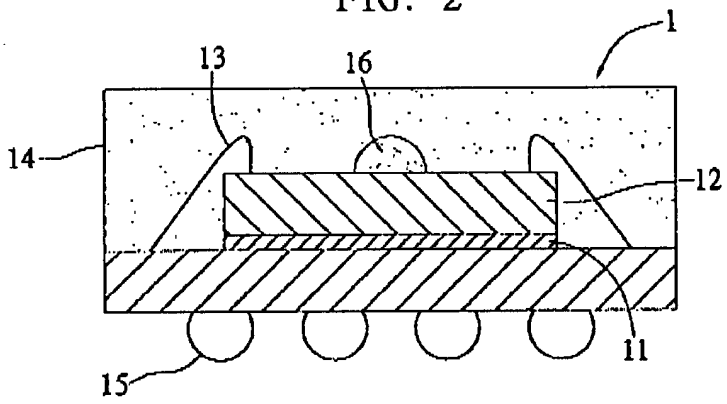
FIG. 2



As shown in FIG. 2, chip 12 is mounted on chip carrier 10, and crack-preventing member 16 is attached to an opposite side of the chip 12.

This arrangement of the crack-preventing member can yield significant benefits. The crack-preventing member 16 is formed as a dam structure such that during a molding process, tension stress applied on the chip 12 from the substrate 10 can be counteracted by compression stress produced by the crack-preventing member 16 situated on the opposite side of the chip 12, thereby preventing the formation of cracks in the chip 12.

Claims 1 and 6-15 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,818,103 to Harada. Claims 1, 2, 4, 6, and 11-15 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 6,144,107 to Narita. Claims 2-5 were rejected under 35 USC 103(a) as being unpatentable over Harada. These rejections are respectfully traversed.

Harada fails to teach or suggest a crack-preventing member situated substantially on an opposite side of a chip with respect to a chip carrier. In Harada, a lead frame 2 includes a mounting portion formed with a groove 5, and a semiconductor chip 1 is attached to the mounting portion by means of a mounting material 3 adapted to fill the groove 5. The groove allows the mounting material to be thickened and thereby reduces thermal stress during evaluation and testing of the device (see column 2, lines 54-57).

In Harada, the lead frame 2 itself functions as the chip carrier and therefore is **not** situated on an opposite side of the chip with respect to the chip carrier, as required in the Applicants' claimed invention. Moreover, the arrangement in Harada does not generate compression stress on the chip to counteract tension stress produced from the chip carrier, as recited in claim 1. The chip carrier and groove in Harada form a different structure performing a different function (i.e., allowing mounting material to be thickened to reduce tension stress) as compared to the Applicants' claimed invention. Therefore, Harada cannot anticipate or otherwise render obvious the Applicants' claimed invention.

Narita also fails to teach or suggest a crack-preventing member situated substantially on an opposite side of a chip with respect to a chip carrier. In Narita, a solid package 6 is provided having a CCD chip 3 mounted on an island member 1a of a lead frame by an adhesive 7, whereby the CCD chip 3 is first encapsulated by a transparent covering member 5 that covers all surfaces of the CCD chip 3 except the surface attached to the island member 1a, so as to enhance heat resistance of the package.

The transparent covering member 5 of Narita encapsulates the CCD chip and the island member portion of the lead frame. In contrast, the Applicants' claimed invention requires that a crack-preventing member is situated substantially on an opposite side of the chip with respect to the chip carrier. In Narita, the transparent covering member 5 is not situated on an opposite side of the chip, but instead surrounds and encloses the chip. Moreover, the transparent covering member 5 is used to moderate stress between the CCD chip 3 and the solid package 6 (see column 6, lines 4-12), whereas the crack-preventing member recited in the Applicants' claimed invention is for generating compression stress to counteract tension stress produced from the chip carrier.

For the reasons discussed above, the Harada and Narita references do not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The first paragraph on page 7 has been amended as follows:

As shown in the drawings, the semiconductor package 3 of the second embodiment of the invention is structurally similar to that of the first embodiment, with the only difference in employing a lead frame [20] 30 with no die pad as a chip carrier for accommodating a chip 32 in the semiconductor package 3. With no provision of a die pad in the lead frame 30, the chip 32 is directly adhered onto leads 30a of the lead frame 30 by means of a tape 31. This reduces contact area between the chip 32 and the lead frame 30, and thus the lead frame 30 and tape 31 would generate relatively smaller tension stress to the chip 32.

IN THE CLAIMS

Claim 1 has been amended as follows:

1. (Amended) A semiconductor package with a crack-preventing member, comprising:

a chip carrier;

at least a chip mounted on the chip carrier and [electrical] electrically connected to the chip carrier;

at least a crack-preventing member formed at a predetermined position on the chip and situated substantially on an opposite side of the chip with respect to the chip carrier, for generating compression stress on the chip to counteract tension stress produced from the chip carrier on the chip in a molding process, so as to prevent the chip from cracking; and

an encapsulant for encapsulating the chip and the crack-preventing member.